REMARKS

Applicant gratefully acknowledges that the examiner has indicated that claims 2-9 contain allowable subject matter. Claims 2-9 have accordingly been rewritten as new claims 15-22.

Claims 13 and 14 have been cancelled.

Claims 1 and 11 stand rejected as being obvious in view of Ueno.

In connection with claims 1 and 11 the examiner has stated that "load board" is a broad term that could refer to a variety of devices including the LSI under test (FIG 16, 22) of Ueno. A search of the PTO data base reveals 10 patents with the term "load board" in the title, all relating to integrated circuit testing. Applicant submits that the term "load board" in context with an integrated circuit tester is well understood in the art to mean a printed circuit board used as an interface between a tester and a device under test, and therefore that Ueno's LSI under test (22) can not properly be construed as a load board.

Claims 1 and 11 have been amended to incorporate limitations from cancelled claim 14, specifically that the conductive switch element is in either electrically conductive contact with, or electrically isolated from, a plurality of contact pins, as opposed to one or more contact pins as detailed in the original claims. In the "second position", as defined in claim 1 for example, the switch element creates a short circuit between all of the contact pins and any other electrically conductive path the switch element is in contact with. In the preferred embodiment of the invention the switch element short circuits each of the contact pins to electrical ground.

Ueno teaches an integrated circuit tester (FIG 16, 24) for testing unpackaged LSI chips (22), the tester featuring a plurality of contact pins (B1-B10) connected to a plurality of tester resources through a plurality of switches (S1-S10), where each contact pin is connected to a single switch and each switch is connected to a single tester resource. Assuming the contact pins of Ueno are separated from each other by a distance that is less than the spacing between pads (23a-23d) on the various LSI chip designs. This combination of features is advantageous for use in an environment where a variety of unpackaged LSI chips are to be tested, as the tester will be compatible with a variety of LSI topologies.

As an example, consider two contact pins (B1 and B2) both of which are in electrically conductive contact with a single pad (23a) of the LSI circuit (22). One contact pin's (B1) associated switch (S1) is open and the switch (S2) associated with the second contact pin (B2) is closed, ensuring that the pad (23a) of the LSI chip (22) is electrically connected to only one tester resource. If the contact pin's associated switches (S1 and S2) were replaced by direct, electrically conductive, connections, there would be an electrical short circuit between the tester resources connected to the two contact pins (B1 and B2). At best this would cause inaccurate test results and at worse both the LSI chip (22) and the tester (24) could be damaged.

However, if the tester (24) is used to test a second LSI chip (not shown) with a different pattern of contact pads, it may be that the two contact pins (B1 and B2) are in electrically conductive contact with two distinct contact pads (not shown) and thus it may be advantageous for both switches (S1 and S2) to be closed.

The above example is intended to show that, in order to function as intended, Ueno requires that there be independent control over which contact pins are connected to the tester and which are not. Such functionality could not be achieved using a single switch element to short circuit all the contact pins. Considering Ueno as a whole, there is nothing to lead a person of ordinary skill in the art to conclude that a switch element that makes electrical contact with a plurality of contact pins, as recited in claims 1 and 11, would improve the design of Ueno. Therefore applicant submits that amended claims 1 and 11 are patentable over Ueno.

Claims 12, 13 and 14 stand rejected as being anticipated by Sokolich. Applicant believes that the examiner was incorrect in including claim 14 in the anticipation rejection, as, unlike claims 12 and 13, claim 14 is dependent on claim 1.

A claim is anticipated only if each and every element recited in the claim is also found in the reference. Among other features, claim 12 recites a contact pin block, at least two contact pins mounted in the contact pin block and a displaceable switch element also mounted in the contact pin block. Thus, for Sokolich to anticipate claim 12, Sokolich must also teach a contact pin block, at least two contact pins mounted in the contact pin block and a displaceable switch

element also mounted in the contact pin block. The lack of any of the aforementioned elements would, by definition, preclude an anticipation rejection.

The examiner has stated that the insulating plate (10) and contact assemblies (32) of Sokolich are analogous, respectively, to the contact pin block and contact pins of claim 12 and that the plurality of switches (C1-10, B1-10) in Sokolich are equivalent to the displaceable switch element (while the examiner cited reference 15 in Sokolich as the counterpart of the contact pins of claim 12, applicant believes that this was in error, as reference 15 pertains only to the backend of the contact assemblies (32)). It is clear however, from examination of Sokolich's specification and accompanying figures, that none of the switches (C1-C10, B1-B10) are mounted in the insulating plate (10). Consequently Sokolich does not disclose each and every element found in claim 12. Therefore Sokolich does not anticipate claim 12.

Furthermore, applicant believes that the arguments presented above regarding claims 1 and 11 also apply to amended claim 12. Applicant therefore submits that claim 12 is patentable.

Respectfully submitted,

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